IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently amended) A method, comprising:

processing tasks associated with at least one processor, wherein the processor comprises at least one cache memory having data stored therein;

transferring at least a portion of the data of the cache memory to another location; and

removing ~~the processor~~ a board including the processor and the cache memory from a system in response to transferring at least the portion of the data from the cache memory to another location, while the system is in operation;

wherein said processing tasks includes sending an acknowledgement signal indicating that it is safe to remove the board from the system.

2. (Original) The method of claim 1, wherein transferring at least the portion of the data of the cache memory to another location comprises transferring at least the portion of the data of the cache memory to non-cache memory in the system.

3. (Original) The method of claim 2, the system comprising a domain defined therein, wherein transferring at least the portion of the data comprises transferring at least the portion of the data of the cache memory of the domain to non-cache memory of the domain in the system.

4. (Cancelled)

5. (Currently amended) The method of claim [[4]] 1, wherein removing the board comprises removing the board from the domain in the system.

6. (Original) The method of claim 1, wherein processing the tasks associated with the at least one processor comprises stopping new tasks from being assigned to the processor.

7. (Original) The method of claim 6, wherein processing the tasks comprises allowing the processor to substantially complete current tasks.

8. (Original) The method of claim 7, wherein processing the tasks comprises flushing the current state of the processor.

9. (Cancelled)

10. (Original) The method of claim 8, wherein transferring at least a portion of the data comprises transferring all of the data stored in the cache memory.

11. (Currently amended) An apparatus, comprising:

at least one processor to execute one or more assigned tasks, wherein the processor includes at least one associated cache memory element having data stored therein; and

an interface to couple the apparatus to a system, wherein the apparatus is adapted to be removed from the system in response to executing the one or more assigned tasks and in response to transferring a portion of the data of the cache memory to a non-cache memory external to the apparatus, while the system is in operation;

wherein the processor is configured to send an acknowledgement signal indicating that it is safe to remove the apparatus from the system.

12-13. (Cancelled)

14. (Currently amended) The apparatus of claim [[13]] 11, wherein the portion of the data comprises all the data stored in the cache memory.

15. (Original) The apparatus of claim 11, wherein the processor is adapted to transmit a

signal to the system when the processor has substantially completed the one or more assigned tasks.

16. (Currently amended) A system, comprising:

an interface adapted to receive a first processor and an associated cache memory;

a control unit adapted to cause at least a portion of the contents of the associated cache memory to be transferred to a second memory location and, in response to the transfer, the first processor to be removed from a domain of the system, while the system is in operation;

wherein the domain comprises at least a second processor that continues to operate for at least a selected duration after the removal of the first processor;

wherein the second processor is further adapted to stop the assignment of additional tasks to the first processor.

17. (Cancelled)

18. (Currently amended) The system of claim [[17]] 16, wherein the second memory location comprises a non-cache memory in the domain.

19. (Cancelled)

20. (Currently amended) The system of claim [[19]] 16, wherein the second processor is further adapted to allow the first processor to substantially complete current tasks.

21. (Original) The system of claim 20, wherein the second processor is adapted to reassign current tasks.

22. (Original) The system of claim 21, wherein the second processor is adapted to flush the current state of the first processor.

23. (Currently amended) A system, comprising:

a first board ~~having~~ including a processor and a memory element;

a second board ~~having~~ including a processor and ~~only~~ a cache memory element, wherein the processor is adapted to execute one or more current tasks;

a control unit adapted to receive an indication to dynamically remove the second board from a domain of the system, wherein the control unit, in response to receiving the indication, is adapted to process at least one current task associated with the processor and transfer at least a portion of data stored in the cache memory on the second board to the memory element on the first board;

wherein, in response to receiving the indication, the control unit is configured to stop the assignment of additional tasks to the processor of the second board.

24. (Original) The system of claim 23, wherein the control unit is adapted to allow the processor on the second board to complete the one or more current tasks.

25. (Currently amended) The system of claim 24, ~~wherein the first board comprises a processor and~~ wherein the control unit is adapted to reassign at least one of the current tasks associated with the processor of the second board to the processor of the first board.

26. (Original) An apparatus, comprising:

at least two processors, wherein each processor has at least one associated cache memory but no non-cache memory;

an address repeater coupled to the two processors, wherein the address repeater is adapted to receive at least one data request and to provide the request to at least one of the two processors;

a data crossbar;

a dual CPU data switch coupled to the two processors and the data crossbar, wherein the dual CPU data switch is adapted to provide data from at least one of the cache memories of the two processors to the data crossbar in response to the received data request; and

a data controller coupled to the data crossbar, wherein the data controller is adapted to indicate to the data crossbar where to send the requested data.

27. (Original) The apparatus of claim 26, wherein at least one of the two processors is adapted to send data address requests through the address repeater and receive the requested data through the data crossbar and dual CPU data switch.

28. (Currently amended) An article comprising one or more machine-readable storage media containing instructions that when executed enable a processor to:

process tasks associated with the processor, wherein the processor comprises at least one cache memory having data stored therein;

transfer at least a portion of the data of the cache memory to another location; ~~and~~

allow ~~the processor~~ a board including the processor and the cache memory to be removed from a system in response to transferring at least the portion of the data from the cache memory to another location, while the system is in operation; and

send an acknowledgement signal indicating that it is safe to remove the board from the system.

29. (Original) The article of claim 28, wherein the instructions when executed enable the processor to transfer at least the portion of the data of the cache memory to non-cache memory in the system.

30. (Original) The article of claim 29, wherein the instructions when executed enable the processor to transfer at least the portion of the data of the cache memory of the domain to non-cache memory of the domain in the system.

31. (Cancelled)

32. (Original) The article of claim 31, wherein the instructions when executed enable the processor to allow the board to be removed from a domain in the system.